layer of copper using electroless plating includes filling the second number of conductor line openings to a top surface of the second patterned photoresist layer.

19. (Amended) The method of claim 13, wherein depositing the second patterned photoresist layer which defines a second number of conductor line openings includes a third number of first level metal line openings.

20. (Amended) A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer on a substrate;

patterning a first photoresist layer over the first seed layer to define a first number of via holes opening to the first seed layer;

forming a first level of copper vias in the first number of via holes using electroless plating;

depositing a second seed layer on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a second number of conductor line openings to the second seed layer;

forming a first level of conductor lines in the second number of conductor line openings using electroless plating;

depositing a third seed layer on the first level of conductor lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a third number of via holes opening to the third seed layer; and

forming a second level of copper vias in the third number of via holes using electroless plating.

21. (Amended) The method of claim 20, wherein the method further comprises:

depositing a fourth seed layer on the second level of copper vias and third photoresist layer;

patterning a fourth photoresist layer over the fourth seed layer to define a fourth number

of conductor line openings to the fourth seed layer; and

forming a second level of conductor lines in the fourth number of conductor line openings using electroless plating.

24. (Amended) The method of claim 21, wherein forming a first level of copper vias in the third number of via holes using electroless plating includes forming the third number of copper vias on the seed layer but not on the first photoresist layer.

28. (Amended) A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate using a physical vapor deposition process;

patterning a first photoresist layer over the first seed layer to define a first number of via holes opening to the first seed layer;

forming a first level of copper vias in the first number of via holes using electroless plating;

depositing a second seed layer on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a second number of conductor line openings to the second seed layer;

forming a first level of copper lines in the second number of conductor line openings using electroless plating;

depositing a third seed layer on the first level of copper lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a third number of via holes opening to the third seed layer;

forming a second level of copper vias in the third number of via holes using electroless plating; and

removing the first, second, and third photoresist layers using oxygen plasma etching.

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34. (Amended) A method for forming a multilayer copper wiring structure, comprising:

depositing a first seed layer including a thin film of Palladium (Pd) or Copper (Cu) on a substrate;

patterning a first photoresist layer over the first seed layer to define a first number of via holes opening to the first seed layer;

forming a first level of copper vias in the first number of via holes using electroless plating;

depositing a second seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the first level of copper vias and first photoresist layer;

patterning a second photoresist layer over the second seed layer to define a second number of conductor line openings to the second seed layer;

forming a first level of copper lines in the second number of conductor line openings using electroless plating;

depositing a third seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the first level of copper lines and the second photoresist layer;

patterning a third photoresist layer over the third seed layer to define a third number of via holes opening to the third seed layer; and

forming a second level of copper vias in the third number of via holes using electroless plating;

depositing a fourth seed layer including a thin film of Palladium (Pd) or Copper (Cu) on the second level of copper vias and third photoresist layer;

patterning a fourth photoresist layer over the fourth seed layer to define a fourth number of conductor line openings to the fourth seed layer; and

forming a second level of copper lines in the fourth number of conductor line openings using electroless plating.

40. (Amended) The method of claim 39, wherein the further includes forming a thin diffusion barrier on the first number of via holes and on the [second] third number of via holes [copper vias] and on the first level and the second level of copper lines.

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